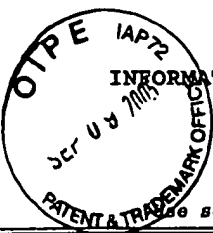
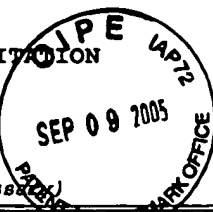
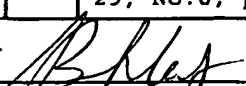
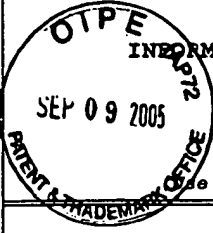



Form PTO-1449 <div style="display: flex; justify-content: space-around; align-items: center;"> <div style="text-align: center;">  </div> <div style="text-align: center;">  </div> </div> <p style="text-align: center;">INFORMATION DISCLOSURE CITATION IN AN APPLICATION</p> <p style="text-align: center;">Use several sheets if necessary</p>				Atty Docket No. P-5404		Serial No. 09/982,458	
Applicant(s) Manjunath Haritsa et al.				Filing Date October 17, 2001		Group 2825	
U.S. PATENT DOCUMENTS							
EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE	
B5	AA	5,387,885	02/07/95	Chi	333	100	
	AB	5,467,040	11/14/95	Nelson et al.	327	276	
	AC	5,581,473	12/03/96	Rusu et al.	364	490	
	AD	5,644,498	07/01/97	Joly et al.	364	489	
	AE	5,656,963	08/12/97	Masleid et al.	327	297	
	AF	5,778,216	07/07/98	Venkatesh	395	558	
	AG	5,864,487	01/26/99	Merryman et al.	364	491	
	AH	5,896,055	04/20/99	Toyonaga et al.	327	295	
	AI	5,917,729	06/29/99	Naganuma et al.	364	491	
	AJ	5,963,729	10/05/99	Aji et al.	395	500.06	
	AK	5,974,245	10/26/99	Li et al.	395	500.11	
	B5	AL	5,994,924	11/30/99	Lee et al.	326	93
FOREIGN PATENT DOCUMENTS							
						Translation	
	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	YES	NO
B5	AM	WO 95/34036	12/14/95	PCT			
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)							
B5	AN	B. Lampson et al., "A Processor for a High-Performance Personal Computer", <u>Seventh Annual Symposium on Computer Architecture</u> , IEEE, pages 146-160, May 1980.					
	AO	C-S Wu et al., "An Automatic Cell Characterization Environment for Cell-Based Design Methodology", IEEE, pages 326-329, May 1993.					
	AP	H. Fair et al., "Clocking Design and Analysis for a 600MHz Alpha Microprocessor", <u>IEEE International Solid State Circuits Conference</u> , IEEE, vol. 41, pages 398-399, 473, February 1998. (XP000862228).					
	AQ	J. Burkis, "Clock Tree Synthesis for High Performance ASICs", IEEE, pages 9-8.1 - 9-8.3, August 1991.					
B5	AR	P. Larsson et al., "Impact of Clock Slope on True Single Phase Clocked (TSPC) CMOS Circuits", <u>IEEE Journal of Solid-State Circuits</u> , IEEE, Vol. 29, No. 6, pages 723-726, June 1994.					
Examiner 			Date Considered 10/28/05				
EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant(s).							

Form PTO-1449				Atty Docket No. P-5404		Serial No. 09/982,458		
				Applicant(s) Manjunath Haritsa et al.				
				Filing Date October 17, 2001		Group 2825		
(Use several sheets if necessary)								
U.S. PATENT DOCUMENTS								
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE	
B	AA	6,088,254	07/11/00	Kermani	365	63		
	AB	6,204,713	03/20/01	Adams et al.	327	295		
	AC	6,205,572	03/20/01	Dupenloup	716	5		
	AD	6,260,182	07/10/01	Mohan et al.	716	12		
	AE	6,263,478	07/17/01	Hahn et al.	716	10		
	AF	6,289,412	09/11/01	Yuan et al.	711	11		
	AG	6,289,498	09/11/01	Dupenloup	716	18		
	AH	6,378,080	04/23/02	Anjo et al.	713	500		
	AI	6,442,740	08/27/02	Kanamoto et al.	716	6		
	AJ	6,457,159	09/24/02	Yalcin et al.	716	6		
	AK	2003/0074175	04/17/03	Haritsa et al.	703	19		
	AL	2003/0074643	04/17/03	Schmitt et al.	716	6		
	AM							
FOREIGN PATENT DOCUMENTS								
							Translation	
		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	YES	NO
	AN							
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)								
B	AO	P.J. Restle et al., "A Clock Distribution Network for Microprocessors", 2000 Symposium on VLSI Circuits, IEEE, pages 184-187, April 2000.						
B	AP	R.B. Mueller-Thuns et al., "Parallel Switch-Level Simulation for VLSI", Proceedings of the European Conference on Design Automation, IEEE, pages 324-328, February 1991. (XP010093616).						
B	AQ	S. Boon et al., "High Performance Clock Distribution for CMOS ASICs", Custom Integrated Circuits Conference, IEEE, pages 15.4.1 - 15.4.5, May 1989. (XP010082184).						
B	AR	J-S Yim et al., "A Floorplan-based Planning Methodology for Power and Clock Distribution in ASICs", Proceedings ACM/IEEE Conference on Design Automation, ACM, pages 766-771, June 1999.						
Examiner 		Date Considered 10/28/05						
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